**California State University, Northridge College of Engineering & Computer Science Electrical and Computer Engineering Department**

**ECE 443L Digital Electronics Laboratory Report 3**

**CMOS Transistor Level Amplifier Design, Simulation and Experimental Test as well as Analysis**

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Abstract:

After designing any CMOS transistor level differential amplifier. We needed to model it after certain specifications. These specifications are as follows. V offset needs to be around 3V with a frequency in the range of 20 kHz to 50kHz. The input voltage needs to be between 10mV and 50mV. We also need to have three different voltages as well as three different frequencies.

Introduction:

The CMOS transistor level differential amplifier is an amazing device. The earth would not be what it is today without it! The CMOS transistor level differential amplifier topology is as shown.

Diagram, schematic

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If this view was not enough to understand the topology of the wonderful CMOS device then another look is offered here.

Diagram, schematic

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In this lab it is required to simulate this differential amplifier under the given constraints.

**Lab 3: CMOS Transistor Level Utility Amplifier Design**

Diagram, schematic

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Case 1: VAMPL of 45mV with a frequency of 20kHz. AV =39.45

Chart, line chart

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Graph of Case 1 with an AV of 39.45 and Frequency of 20kHz with double bias NMOS

Diagram

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Case 3 VAMPL 10mV @ 20Khz

Chart, line chart

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Table

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Graphical representation of case 3 with an AV of 74.95 and Triple NMOS

Diagram, schematic

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Case 5 Quadruple NMOS with VAMPL of 21mV @ 40kHz

Chart, line chart

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Table

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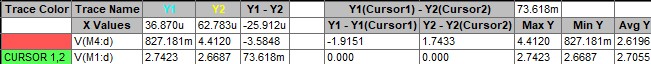
Case 5 Graphical representation of an AV of 110.16

**Lab 3: CMOS Transistor Level Utility Amplifier Design**Diagram, schematic

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Chart

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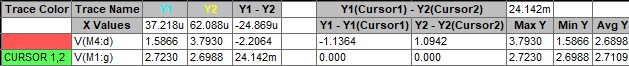
Graphical user interface, chart, application

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Figure 3.2: CMOS Transistor Amplifier Waveform and Cursor with Double Sizing and A(v) @ 48.38V

Figure 3.3: CMOS Transistor Amplifier Design with Triple Sizing and V(m) @ 35mV and Freq @ 25kHzDiagram, schematic

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Figure 3.4: CMOS Transistor Amplifier Waveform and Cursor with Triple Sizing and A(v) @ 67.27VChart

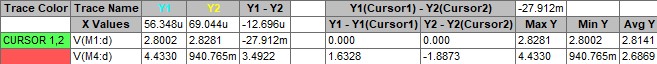
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Chart

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Figure 3.6: CMOS Transistor Amplifier Waveform and Cursor with Quadruple Sizing and A(v) @ 125.9V

Conclusion:

This lab gave us the opportunity to understand the effects that certain sizing of NMOS transistors have on amplification properties of CMOS circuits. This lab is very important and needs to be taught all over the globe. This lab allowed for better understanding of how CMOS transistors function under certain constraints that were given in this lab.